Note about $\Delta\Sigma$ ADC Front-End for Condenser Microphones

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1 Introduction

The following might well be a rather old shoe; comments welcome.

The conventional DC-biased operation of analog condenser microphones has the beauty, that only the small AC voltage given by capacitance variation of the capsule appears at the buffer amplifier; the large DC bias is normally removed by a coupling capacitor.

It would be nice, if the microphone capsule ($\approx 40 \ldots 90\,\mathrm{pF}$) could be directly included into the $\Delta\Sigma$ ADC front-end, so that it is operated at the ADC's oversampling frequency. Then the classical DC bias ($\approx 30 \ldots 200\,\mathrm{V}$) circuitry and buffer amplifier would be obsolete.

One main problem of such a scenario might be, that the full charge (bias $\approx 3.3 \ldots 10\,\mathrm{V}$ by ADC plus small variation by sound) would have to be handled by the ADC front-end. This total charge is about two orders of magnitude larger than the charge variation by sound alone. The first integrator amplifier of the $\Delta\Sigma$ ADC might easily be over-driven by these large charges. Or, the full-scale charge of the ADC is determined by the bias charge of the capsule, so that the useful conversion range for sound signals is only a small fraction of this.

The following might be one method to remove the bias charge by *passive* balancing, involving MOS switches only, so that only the signal charge of the capsule is given to the ADC front-end integrator.

If it is useful for capsules with single membranes/capacitors, it could be extended for dual-membrane capsules, with digitally presettable directional pattern.

A problem might be, that the source capacitance (still about *half* the capsule capacitance) seen by the ADC front-end integrator might negatively influence its settling and noise behavior.

2 Capacitors

Capacitor C_1 is variable (e. g. microphone capsule) and C_2 is reference capacitor (e. g. fixed or 2nd capsule). The small capacitance variation is δ.

$$C_1 = C_2 \cdot (1 + \delta) \tag{1}$$

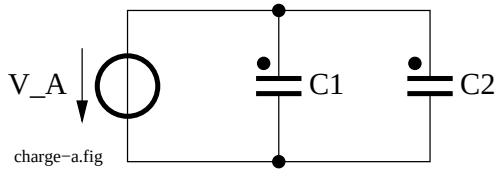
3 Sequence

The charge from the variation δ of capacitor C_1 is dumped into the ADC front-end in a periodic three-step sequence, running at oversampling frequency:

3.1 Charging

Both capacitors C_1 and C_2 are connected in parallel and charged to the same voltage V_A, which is derived from or equal to the ADC's reference voltage.

In the following, MOS switches are not shown, all switch resistances are ignored, transitional guarding steps are left out, and complete charge settling is always presupposed.



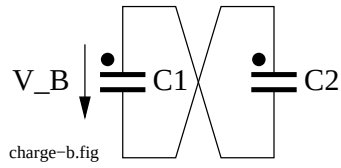
$$V_{1A} = V_{2A} = V_A \tag{2}$$

The capacitors carry the charges Q_{1A} and Q_{2A}.

$$Q_{1A} = C_1 \cdot V_A = C_2 \cdot (1 + \delta) \cdot V_A \tag{3}$$
$$Q_{2A} = C_2 \cdot V_A \tag{4}$$

3.2 Balancing

Capacitor C_2 is now reversely connected to C_1. A balancing charge ΔQ_A brings the capacitors into equilibrium voltage V_B.



$$V_{1B} = -V_{2B} = V_B \tag{5}$$

They now carry charges Q_{1B} and Q_{2B}. The charge balance equations are:

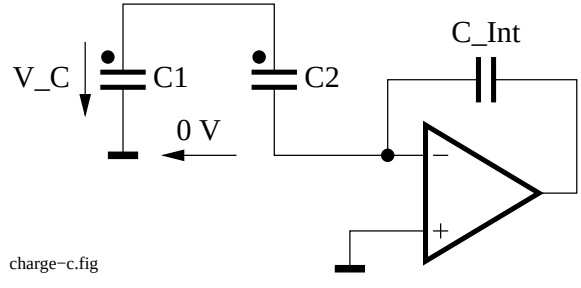
$$\begin{aligned} Q_{1B} = Q_{1A} - \Delta Q_A &= C_1 \cdot V_B & (6)\\ Q_{2B} = Q_{2A} - \Delta Q_A &= -C_2 \cdot V_B & (7) \end{aligned}$$

Subtracting equations gives:

$$\begin{aligned} Q_{1A} - Q_{2A} &= (C_1 + C_2) \cdot V_B & (8)\\ \delta Q_{2A} &= C_2 \cdot (2+\delta) \cdot V_B & (9)\\ V_B &= V_A \cdot \frac{\delta}{2+\delta} & (10) \end{aligned}$$

3.3 Dumping

Capacitor C_2 is now connected between the grounded capacitor C_1 and the integrator amplifier input at virtual ground. A balancing charge ΔQ_B brings them into equilibrium voltage V_C.



$$V_{1C} = V_{2C} = V_C \tag{11}$$

They now carry the charges Q_{1C} and Q_{2C}. The charge balance equations are:

$$\begin{aligned} Q_{1C} = Q_{1B} - \Delta Q_B &= C_1 \cdot V_C & (12)\\ Q_{2C} = Q_{2B} + \Delta Q_B &= C_2 \cdot V_C & (13) \end{aligned}$$

Dividing equations gives:

$$\frac{Q_{1B} - \Delta Q_B}{Q_{2B} + \Delta Q_B} = \frac{C_1}{C_2} \tag{14}$$

$$-\Delta Q_B \cdot (C_2 + C_1) = C_1 \cdot Q_{2B} - C_2 \cdot Q_{1B} \tag{15}$$

$$\Delta Q_B = \frac{C_2 \cdot C_2 \cdot (1+\delta) \cdot V_B + C_2 \cdot (1+\delta) \cdot C_2 \cdot V_B}{C_2 \cdot (2+\delta)} \tag{16}$$

$$\Delta Q_B = V_B \cdot C_2 \cdot \frac{2 \cdot (1+\delta)}{2+\delta} \tag{17}$$

$$\Delta Q_B = V_A \cdot C_2 \cdot \frac{2\delta \cdot (1+\delta)}{(2+\delta)^2} \tag{18}$$

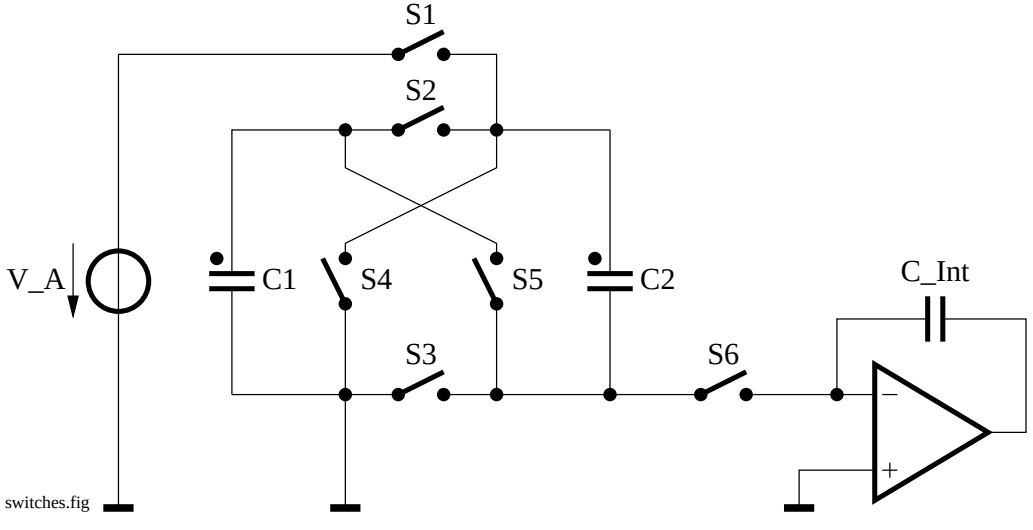
For small $|\delta| \ll 1$ (e. g. normal microphone operation) this is approximately:

$$\Delta Q_B \approx V_A \cdot C_2 \cdot \frac{\delta}{2} \tag{19}$$

This charge ΔQ_B has to be handled by the ADC. The small remaining charges Q_{1C} and Q_{2C} are useless.

4 Implementation by Switches

The drawing shows one possible implementation by MOS-switches.



The switches are operated as follows:

Phase	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**
Charging	closed	closed	closed	open	open	open
Balancing	open	open	open	closed	closed	open
Dumping	open	closed	open	open	open	closed

In the charging phase, capacitor C_1 is charged through S2 and capacitor C_2 is charged through S3, so that their charging time constants are matched.

5 Unclear Points

- How does non-ideal (e. g. incomplete) balancing step affect performance?
- How are integrator settling and noise influenced by source capacitance?
- Dumping C_1 and C_2 in parallel rather than in series also possible, but worse for noise. Is this so?